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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,458	10/23/2001	Thomas Fung	2875.0440001	6843

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EXAMINER	
POPHAM, JEFFREY D	

ART UNIT	PAPER NUMBER
2137	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/004,458	FUNG ET AL.	
	Examiner	Art Unit	
	JEFFREY D. POPHAM	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-12,14-18,20-24 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-12,14-18,20-24 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Remarks

Claims 1-4, 6-12, 14-18, 20-24, and 26 are pending.

The Examiner believes that an interview may help further prosecution in this application. If, upon reviewing this office action, Applicant's Representative agrees, the Examiner may be reached at the number provided below.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/2/2008 has been entered.

Claim Objections

2. Claims 1-4, 6-12, 14-18, 20-24, and 26 are objected to because of the following informalities:

Each of claims 14 and 26 claim dependence upon a cancelled claim. For purposes of prior art rejection, claim 14 has been construed as being dependent upon claim 12 and claim 26 has been construed as being dependent upon claim 24.

All of the claims appear to have the issue of conditional statements that do not always provide an outcome. Claim 1 provides for processing first and second data

using processing engines, then branches into conditional statements. The first occurs if the first interrupt indicator is enabled and processing of the second data completes. The second occurs if processing of the first data completes before processing of the second data. The third occurs if a second interrupt indicator is enabled. What is unclear is what happens when none of the above conditionals hold true (e.g. when the second data completes processing before the first data and the first and second interrupt indicators are disabled). This is just one example, as the conditionals above are intricate, especially when viewed in light of each other. Claim 15 has the same issues with two conditional statements.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 4, 6-12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaya (U.S. Patent 5,978,830) in view of Yamaura (U.S. Patent 6,175,890) and Ghaffari (U.S. Patent 6,145,017).

Regarding Claim 1,

Nakaya discloses a method for processing data using a plurality of processing engines, the method comprising:

Processing first data associated with a younger control record in a first processing engine (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Processing second data associated with an older control record in a second processing engine (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Generating an interrupt when the processing of the first data is completed if a first interrupt indicator in the younger control record has been issued and processing of the second data has been completed (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Moving the first interrupt indicator associated with the younger control record onto a second interrupt indicator associated with the older control record if processing of the first data completes before processing of the second data (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12); and

Generating an interrupt when the processing of the second data is completed (Figure 7; Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12; this could be a serial computing part completing before another serial computing part or a set of parallel computing parts);

But does not explicitly disclose the enablement of a first interrupt indicator in the younger control record, or that generating of the interrupt

when processing of the second data is completed if a second interrupt indicator in the older control record is enabled.

Yamaura, however, discloses enabling a first interrupt indicator in the younger control record (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10). Where the interrupt is placed, whether it be in a register devoted to interrupt indicators and their associations to control records or within the control record itself, is of no significance to this method, since placing the interrupt indicator within the control record does not provide an advantage over using a register to store the indicator. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the parallel job scheduling system of Nakaya in order to efficiently restore data to be communicated to an external processor.

Ghaffari, however, discloses generating an interrupt when the processing of the second data is completed if a second interrupt indicator in the older control record is enabled (Command Chaining field is set) (Column 9, lines 3-25; and Column 10, lines 36-56). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the control flags/fields of Ghaffari into the parallel job scheduling system of Nakaya as modified by Yamaura in order to explicitly designate whether an interrupt must be issued after completion of each command, so as to provide control over the frequency of command

completion interrupts and thereby reduce the number of such interrupts issued and/or to tell the interrupt issuing entity that there are more commands to be executed before issuing the interrupt.

Regarding Claim 3,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 1, in addition, Yamaura discloses that moving the first interrupt indicator comprises determining that the first interrupt indicator is enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Throughout this action, when the moving (or collapsing) of interrupt indicators is cited as being in Yamaura, it is to be understood that Yamaura teaches t he foundations of how it is done, via the enabling and disabling of interrupt indicators within the interrupt controller, while the portions of Nakaya cited above discloses the moving of interrupt indicators (not issuing an interrupt until termination notices from all of the processors are issued).

Regarding Claim 4,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 1, in addition, Nakaya discloses that moving the first interrupt indicator comprises delaying the generation of an interrupt associated with the younger control record (Column 25, lines 40-63). The termination notices are issued at all of the processors before any one of the processors can generate the interrupt.

Regarding Claim 6,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 4, in addition, Yamaura discloses that moving the first interrupt indicator comprises setting the first interrupt indicator associated with the younger control record to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 7,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 6, in addition, Yamaura discloses that moving the first interrupt indicator further comprises setting the second interrupt indicator associated with the older control record to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 8,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 1, in addition, Nakaya discloses that the older control record comprises a reference to data (Column 12, lines 13-29).

Regarding Claim 9,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 8, in addition, Nakaya discloses that the older control record comprises a reference to an operation to be performed on data (Column 12, lines 13-29).

Regarding Claim 10,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 1, in addition, Yamaura discloses writing processed data to memory associated with a host (Column 4, line 59 to Column 5, line 49).

Regarding Claim 11,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 10, in addition, Nakaya discloses that the processing engines are coupled to the interrupt controller (Figure 1); and Yamaura discloses that the external processor is coupled to the interrupt controller (Figure 1).

Regarding Claim 12,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 11, in addition, Nakaya discloses that the external processor is coupled to the processing engines through a scheduler (synchronizer) (Figure 1).

Regarding Claim 14,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 13, in addition, Yamaura discloses that the external processor reads the processed data when the interrupt is generated (Column 4, line 59 to Column 5, line 49).

4. Claims 2, 15-18, 20-24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaya in view of Yamaura and Ghaffari, further in view of Pierson (Pierson et al., "Context-Agile Encryption for High Speed Communication Networks",

Computer Communications Review, Association for Computing Machinery, Vol. 29, No. 1, January 1999, pp. 35-49).

Regarding Claim 2,

Nakaya as modified by Yamaura and Ghaffari does not explicitly disclose that the first processing engine is a public key engine.

Pierson, however, discloses that the first processing engine is a public key engine (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the parallel job scheduling system of Nakaya as modified by Yamaura and Ghaffari in order to allow the system to perform encryption and authentication quickly and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 15,

Nakaya discloses an apparatus comprising:

A first processing engine configured to receive a first control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

A second processing engine configured to receive a second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

A history buffer (interrupt controller/synchronizer) containing information associated with the first and second control records including a first interrupt indicator associated with the first control record and a second interrupt indicator associated with the second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Wherein the history buffer is configured to move the first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record if processing of the first control record completes before processing of the second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Wherein an interrupt is generated when the processing of the second data is completed (Figure 7; Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

But does not explicitly disclose that the apparatus is a cryptography accelerator, an interface coupled to an external processor and memory associated with the external processor, or that generating of the interrupt when processing of the second data is completed if a second interrupt indicator in the older control record is enabled.

Yamaura, however, discloses an interface coupled to an external processor and memory associated with the external processor; the interface being coupled to the processing engines as well (Column 1, lines

12-30; Column 4, line 59 to Column 5, line 10; and Figure 1). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the parallel job scheduling system of Nakaya in order to efficiently restore data to be communicated to an external processor.

Ghaffari, however, discloses that an interrupt is generated when the processing of the second data is completed if a second interrupt indicator in the older control record is enabled (Column 9, lines 3-25; and Column 10, lines 36-56). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the control flags/fields of Ghaffari into the parallel job scheduling system of Nakaya as modified by Yamaura in order to explicitly designate whether an interrupt must be issued after completion of each command, so as to provide control over the frequency of command completion interrupts and thereby reduce the number of such interrupts issued and/or to tell the interrupt issuing entity that there are more commands to be executed before issuing the interrupt.

Pierson, however, discloses that the apparatus is a cryptography accelerator (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the parallel job scheduling system of Nakaya as modified by Yamaura and Ghaffari in order to allow the system to perform encryption and authentication quickly

and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 16,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 15, in addition, Pierson discloses that the first processing engine is a public key engine (Pages 46-48, Section 5.2).

Regarding Claim 17,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 15, in addition, Nakaya discloses that the history buffer is configured to collapse the first interrupt indicator associated with the first control record onto the second interrupt indicator associated with the second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12); and Yamaura discloses that this is performed when the first interrupt indicator is enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 18,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 17, in addition, Nakaya discloses that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises delaying the generation of an

interrupt associated with the first control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12).

Regarding Claim 20,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 18, in addition, Yamaura discloses that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises setting the first interrupt indicator associated with the first control record to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 21,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 20, in addition, Yamaura discloses that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises setting the second interrupt indicator associated with the second control record to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 22,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 15, in addition, Nakaya discloses that the second control record comprises a reference to data (Column 12, lines 13-29).

Regarding Claim 23,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 22, in addition, Nakaya discloses that the second control record comprises a reference to an operation to be performed on data (Column 12, lines 13-29).

Regarding Claim 24,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 23, in addition, Nakaya discloses that the external processor is coupled to the processing engines through a scheduler (synchronizer) (Figure 1).

Regarding Claim 26,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 24, in addition, Yamaura discloses that the external processor reads the processed data when the interrupt is generated (Column 4, line 59 to Column 5, line 49).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY D. POPHAM whose telephone number is (571)272-7215. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571)272-3865. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey D Popham
Examiner
Art Unit 2137

/Jeffrey D Popham/
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